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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/670,797	09/26/2000	William A. Kleinhans	1191	4731

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EXAMINER	
VILLECCO, JOHN M	
ART UNIT	**PAPER NUMBER**
2612	5

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/670,797		
	Examiner	Art Unit	
	John M. Villecco	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) 2,6,12 and 16 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 26 September 2000 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 2, 6, 12, and 16 are objected to because of the following informalities:

   - Regarding ***claims 2, 6, 12, and 16***, applicant discloses that accessing the "third row" or the "N+1+M" row of the array causes the so set the image exposure time of the semiconductor imaging chip. However, it appears that the accessing the row only sets the image exposure time of just that row and not the entire semiconductor imaging chip.

2. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. <u>Claims 4 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Guidash (U.S. Patent No. 6,218,656).</u>

5. Regarding ***claim 4***, Guidash discloses an active pixel sensor arrangement with shared reset signal and row select lines. More specifically, Guidash discloses a plurality of pixel sensors arranged in an array of rows and columns (col. 3, lines 3). Each row of the array has an

access line shared with a reset line of a previous row to form a shared access/reset line which simultaneously access the current row and reset the previous row. The array of pixels includes per column signal processing. This signal processing is identified as correlated double sampling (col. 3, lines 4-13). A reset signal is pulsed and a sample of the reset signal is stored in capacitor, Cr. Then a pixel signal is read out and stored in capacitor, Cs. Then the system selects the next row (N+1) to sample. See column 3, line 45 to column 4, line 30 and Figure 2.

6. As for ***claim 14***, Guidash discloses an active pixel sensor arrangement with shared reset signal and row select lines. More specifically, Guidash discloses a plurality of pixel sensors arranged in an array of rows and columns (col. 3, lines 3). Each row of the array has an access line shared with a reset line of a previous row to form a shared access/reset line which simultaneously access the current row and reset the previous row. The array of pixels includes per column signal processing. This signal processing is identified as correlated double sampling (col. 3, lines 4-13). A reset signal is pulsed and a sample of the reset signal is stored in capacitor, Cr. Then a pixel signal is read out and stored in capacitor, Cs. Then the system selects the next row (N+1) to sample. See column 3, line 45 to column 4, line 30 and Figure 2. Inherently the lines and would be operated by a driver and the driver operated by a scan controller to implement proper timing.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 1, 5, 11, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guidash (U.S. Patent No. 6,218,656, hereinafter referred to as Guidash '656) in view of Guidash (U.S. Patent No. 6,587,146, hereinafter referred to as Guidash '146).**

9. Regarding ***claim 1***, Guidash '656 discloses an active pixel sensor arrangement with shared reset signal and row select lines. More specifically, Guidash '656 discloses a plurality of pixel sensors arranged in an array of rows and columns (col. 3, lines 3). Each row of the array has an access line shared with a reset line of a previous row to form a shared access/reset line which simultaneously access the current row and reset the previous row. The array of pixels includes per column signal processing. This signal processing is identified as correlated double sampling (col. 3, lines 4-13). A reset signal is pulsed and a sample of the reset signal is stored in capacitor, Cr. Then a pixel signal is read out and stored in capacitor, Cs. Then the system selects the next row (N+1) to sample. Using the per column difference amplifier (32), the second sample is subtracted from the first sample forming a corrected output. See column 3, line 45 to column 4, line 30 and Figure 2.

Guidash '656, however, fails to specifically disclose canceling the internal offset voltage of the active pixel sensor. Guidash '146, on the other hand, discloses that it is well known in the art to sample an active pixel sensor a plurality of times to cancel an offset voltage of the pixel sensor. In column 4, lines 60-67, Guidash '146 teaches that the process operates to cancel the pixel source follower offset voltage. Therefore, it would have bee obvious to one of ordinary skill in the art at the time the invention was made to also cancel the offset voltage in Guidash '656 in order to form a better image.

10. As for ***claim 5***, as mentioned above in the discussion of claim 4, Guidash '656 discloses all of the limitations of the parent claim. However, Guidash '656 fails to specifically disclose canceling an internal offset voltage. Guidash '146, on the other hand, discloses that it is well known in the art to sample an active pixel sensor a plurality of times to cancel an offset voltage of the pixel sensor. In column 4, lines 49-67, Guidash '146 teaches that the process operates to cancel the pixel source follower offset voltage by storing first and second pixel samples and subtracting the difference. Therefore, it would have bee obvious to one of ordinary skill in the art at the time the invention was made to also cancel the offset voltage in Guidash '656 in order to form a higher quality image.

11. With regard to ***claim 11***, Guidash '656 discloses an active pixel sensor arrangement with shared reset signal and row select lines. More specifically, Guidash '656 discloses a plurality of pixel sensors arranged in an array of rows and columns (col. 3, lines 3). Each row of the array has an access line shared with a reset line of a previous row to form a shared access/reset line which simultaneously access the current row and reset the previous row. The array of pixels includes per column signal processing. This signal processing is identified as correlated double sampling (col. 3, lines 4-13). A reset signal is pulsed and a sample of the reset signal is stored in capacitor, Cr. Then a pixel signal is read out and stored in capacitor, Cs. Then the system selects the next row (N+1) to sample. See column 3, line 45 to column 4, line 30 and Figure 2. Inherently the lines and would be operated by a driver and the driver operated by a scan controller to implement proper timing.

Guidash '656, however, fails to specifically disclose canceling the internal offset voltage of the active pixel sensor. Guidash '146, on the other hand, discloses that it is well known in the

art to sample an active pixel sensor a plurality of times to cancel an offset voltage of the pixel sensor. In column 4, lines 60-67, Guidash '146 teaches that the process operates to cancel the pixel source follower offset voltage. Therefore, it would have bee obvious to one of ordinary skill in the art at the time the invention was made to also cancel the offset voltage in Guidash '656 in order to form a better image.

12. Regarding ***claim 15***, as mentioned above in the discussion of claim 14, Guidash '656 discloses all of the limitations of the parent claim. However, Guidash '656 fails to specifically disclose canceling an internal offset voltage. Guidash '146, on the other hand, discloses that it is well known in the art to sample an active pixel sensor a plurality of times to cancel an offset voltage of the pixel sensor. In column 4, lines 49-67, Guidash '146 teaches that the process operates to cancel the pixel source follower offset voltage by storing first and second pixel samples in capacitors Cr and Cs and subtracting the difference using the difference amplifier (32). Therefore, it would have bee obvious to one of ordinary skill in the art at the time the invention was made to also cancel the offset voltage in Guidash '656 in order to form a higher quality image.

13. **Claims 2, 3, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guidash (U.S. Patent No. 6,218,656, hereinafter referred to as Guidash '656) in view of Guidash (U.S. Patent No. 6,587,146, hereinafter referred to as Guidash '146) and further in view of Panicacci (U.S. Patent No. 6,529,242)**.

14. Regarding ***claim 2,*** as mentioned above in the discussion of claim 1, both Guidash '656 and Guidash '146 disclose all of the limitations of the parent claim. However, neither of the

aforementioned references discloses accessing a row ahead of the previous rows in order to set an image exposure time, nor even how an exposure time is even set. Panicacci, on the other hand discloses that it is well known in the art to access rows before reading them out in order to begin the integration process (i.e. set exposure time). Panicacci discloses the use of two shutter pulses. The first shutter pulse begins the integration period by releasing the pixels from reset (col. 2, lines 55-56). As shown in Figure 4, as each row is released from reset a previous row is read out. See column 3, lines 1-35. This method serves an efficient way to establish an exposure time in an APS sensor. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to access a third row ahead of the other rows to begin an integration process so that an efficient exposure method is implemented in Guidash.

15. As for ***claim 3***, Panicacci discloses in Figure 4, that as the first pointer releases the row from reset, a different row is read out.

16. ***Claim 12*** is considered substantively equivalent to claim 2. Please see the discussion of claim 2 above.

17. ***Claim 13*** is considered substantively equivalent to claim 3. Please see the discussion of claim 3 above.

18. **Claims 6-9 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guidash (U.S. Patent No. 6,218,656, hereinafter referred to as Guidash '656) in view of Panicacci (U.S. Patent No. 6,529,242)**.

19. Regarding ***claim 6***, as mentioned above in the discussion of claim 4, Guidash '656 discloses all of the limitations of the parent claim. However, Guidash '656 fails to specifically

disclose accessing an N+1+M row of the array to set an image exposure time of the semiconductor imaging chip. Panicacci, on the other hand discloses that it is well known in the art to access rows before reading them out in order to begin the integration process (i.e. set exposure time). Panicacci discloses the use of two shutter pulses. The first shutter pulse begins the integration period by releasing the pixels from reset (col. 2, lines 55-56). As shown in Figure 4, as each row is released from reset a previous row is read out. See column 3, lines 1-35. This method serves an efficient way to establish an exposure time in an APS sensor. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to access a third row ahead of the other rows to begin an integration process so that an efficient exposure method is implemented in Guidash.

20. With regard to ***claim 7***, Panicacci discloses in Figure 4, that as the first pointer releases the row from reset, a different row is read out.

21. As for ***claim 8***, Guidash '656 discloses an active pixel sensor arrangement with shared reset signal and row select lines. More specifically, Guidash '656 discloses a plurality of pixel sensors arranged in an array of rows and columns (col. 3, lines 3). Each row of the array has an access line shared with a reset line of a previous row to form a shared access/reset line which simultaneously access the current row and reset the previous row. The array of pixels includes per column signal processing. This signal processing is identified as correlated double sampling (col. 3, lines 4-13). A reset signal is pulsed and a sample of the reset signal is stored in capacitor, Cr. Then a pixel signal is read out and stored in capacitor, Cs. Then the system selects the next row (N+1) to sample. See column 3, line 45 to column 4, line 30 and Figure 2.

Guidash '656, however, fails to specifically disclose accessing an N+1+M row and setting the image exposure time of the semiconductor imaging chip. Panicacci, on the other hand discloses that it is well known in the art to access rows before reading them out in order to begin the integration process (i.e. set exposure time). Panicacci discloses the use of two shutter pulses. The first shutter pulse begins the integration period by releasing the pixels from reset (col. 2, lines 55-56). As shown in Figure 4, as each row is released from reset a previous row is read out. See column 3, lines 1-35. This method serves an efficient way to establish an exposure time in an APS sensor. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to access a third row ahead of the other rows to begin an integration process so that an efficient exposure method is implemented in Guidash.

22. Regarding ***claim 9***, Panicacci discloses in Figure 4, that as the first pointer releases the row from reset, a different row is read out.

23. ***Claim 16*** is considered substantively equivalent to claim 6. Please see the discussion of claim 6 above.

24. ***Claim 17*** is considered substantively equivalent to claim 7. Please see the discussion of claim 7 above.

25. ***Claim 18*** is considered substantively equivalent to claim 8. Please see the discussion of claim 8 above.

26. ***Claim 19*** is considered substantively equivalent to claim 9. Please see the discussion of claim 9 above.

27. **Claims 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guidash (U.S. Patent No. 6,218,656, hereinafter referred to as Guidash '656) in view of Panicacci (U.S. Patent No. 6,529,242) and further in view of Guidash (U.S. Patent No. 6,587,146, hereinafter referred to as Guidash '146)**.

28. Regarding ***claim 10***, as mentioned above in the discussion of claim 8, both Guidash '656 and Panicacci disclose all of the limitations of the parent claim. However, neither of the aforementioned references discloses canceling an internal offset voltage. Guidash '146, on the other hand, discloses that it is well known in the art to sample an active pixel sensor a plurality of times to cancel an offset voltage of the pixel sensor. In column 4, lines 49-67, Guidash '146 teaches that the process operates to cancel the pixel source follower offset voltage by storing first and second pixel samples in capacitors Cr and Cs and subtracting the difference using the difference amplifier (32). Therefore, it would have bee obvious to one of ordinary skill in the art at the time the invention was made to also cancel the offset voltage in Guidash '656 in order to form a higher quality image.

29. ***Claim 20*** is considered substantively equivalent to claim 10. Please see the discussion of claim 10 above.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 872-9306 (For either formal or informal communications intended for entry. For informal or draft communications, please label "**PROPOSED**" or "**DRAFT**")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington VA, Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M. Villecco whose telephone number is (703) 305-1460. The examiner can normally be reached on Monday through Thursday from 7:00 am to 5:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber, can be reached on (703) 305-4929. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the customer service desk whose telephone number is (703) 306-0377.

JMV
2/26/04

WENDY R. GARBER
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